

FIG. 3

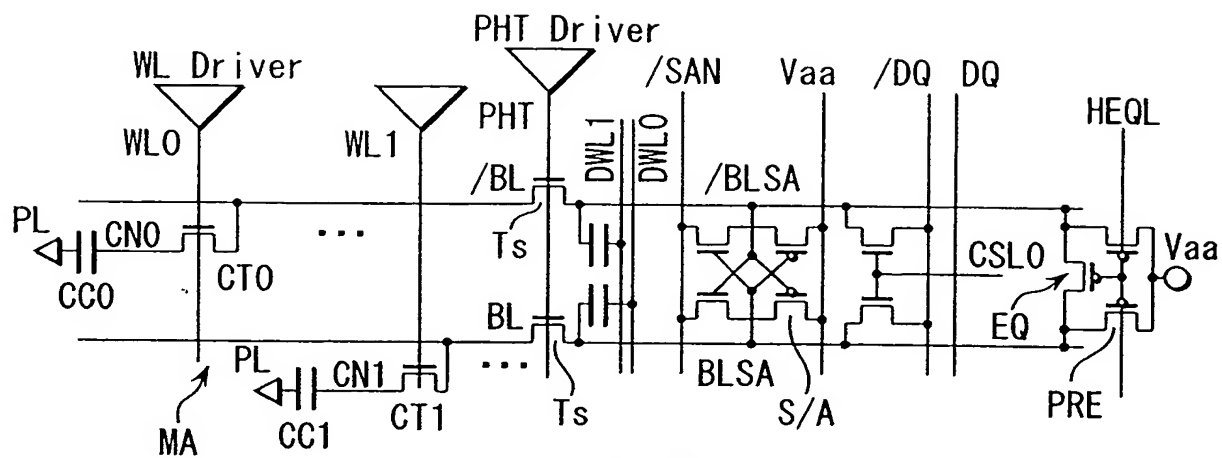


FIG. 4

FIG. 6A

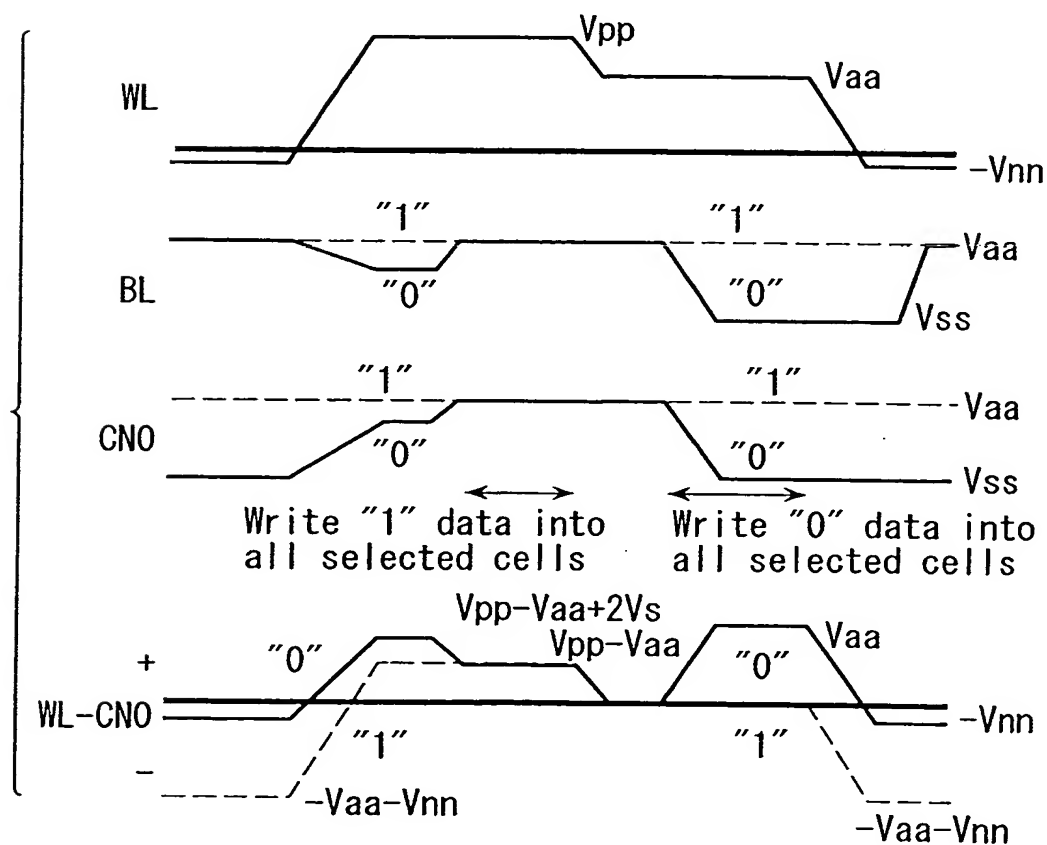
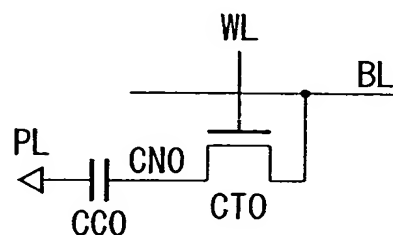
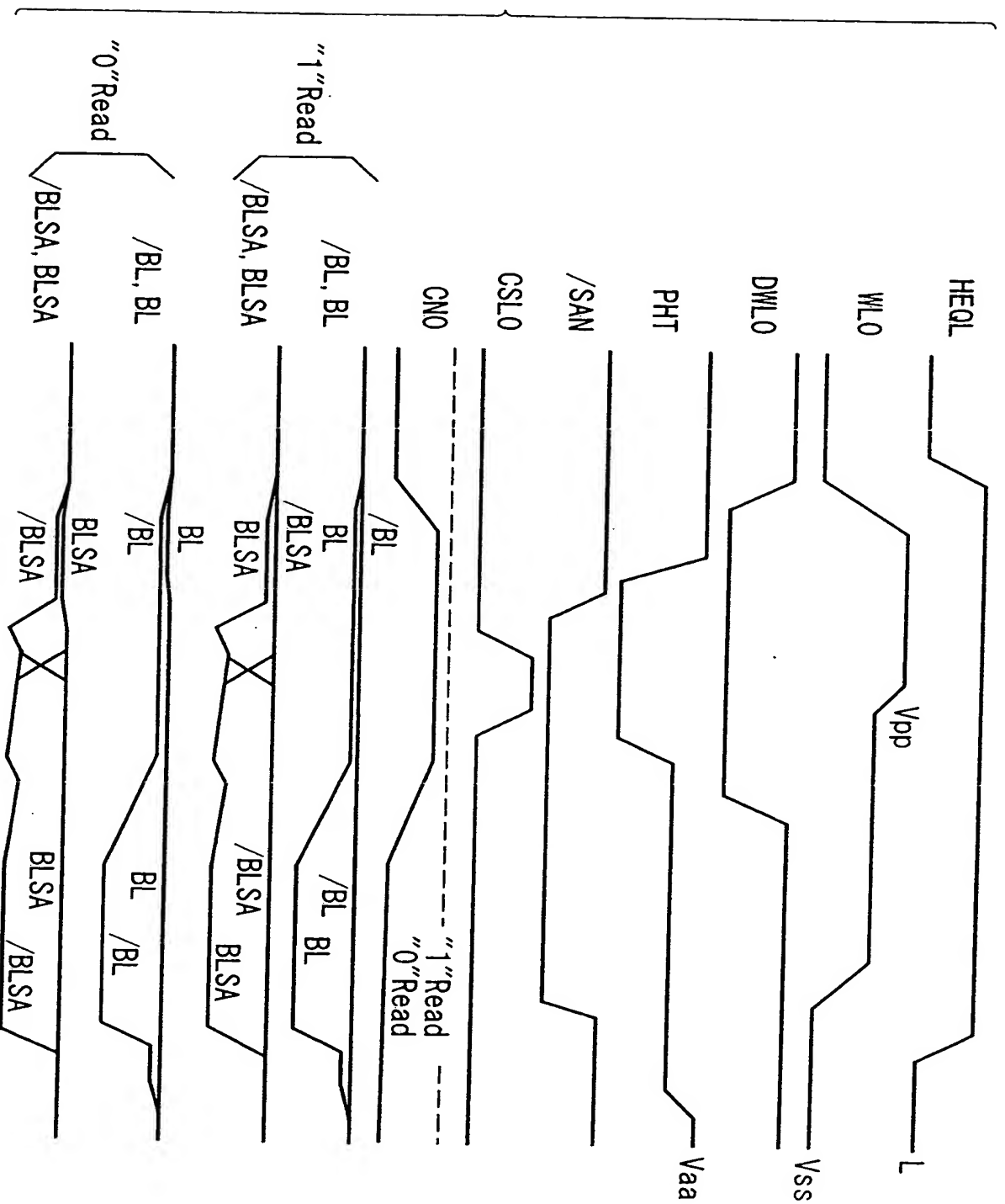


FIG. 6B

FIG. 5



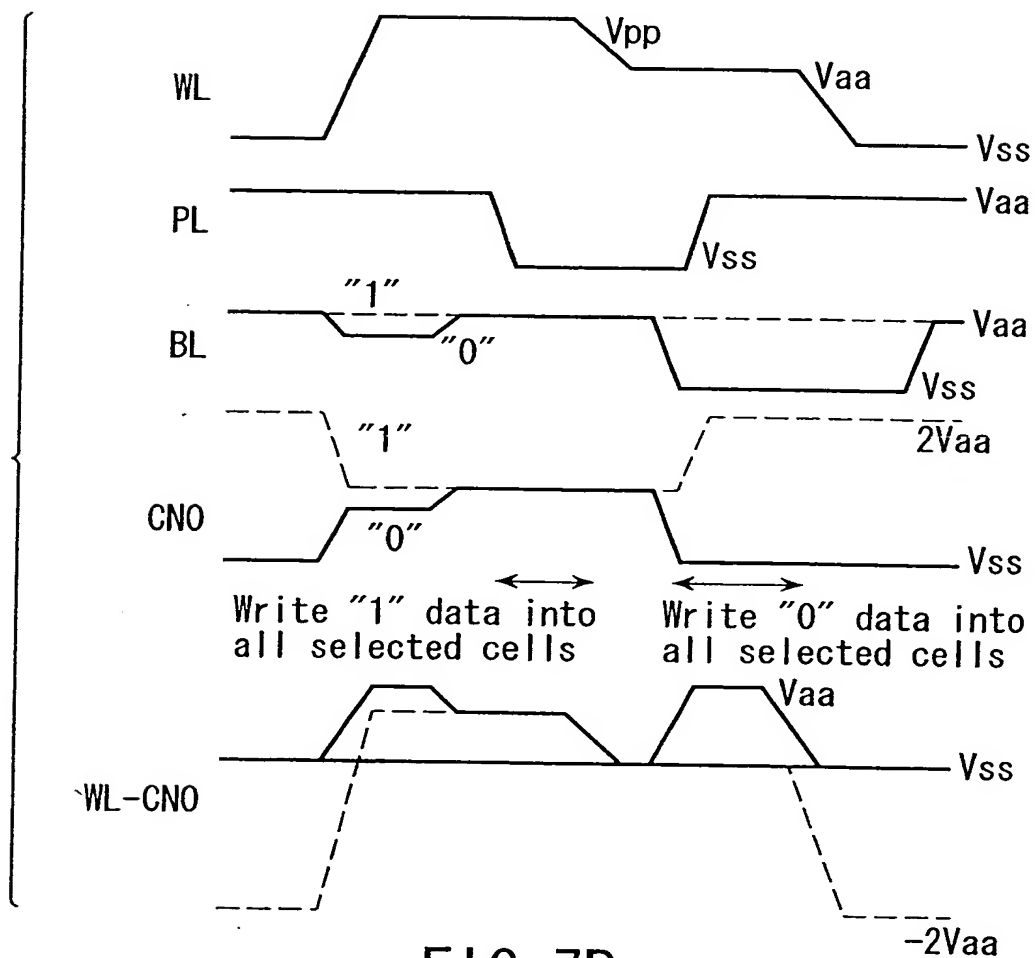
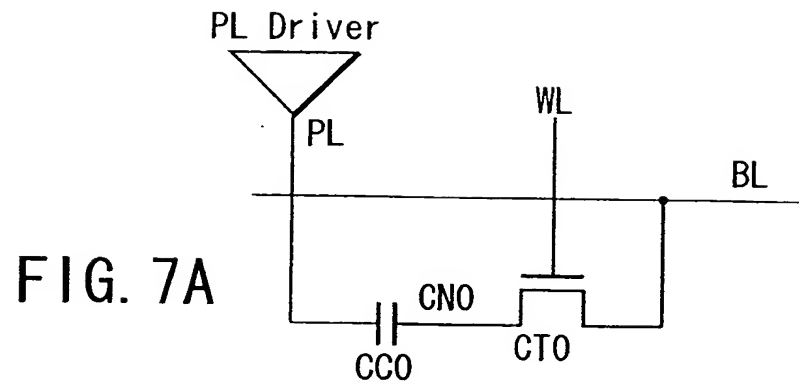


FIG. 8A

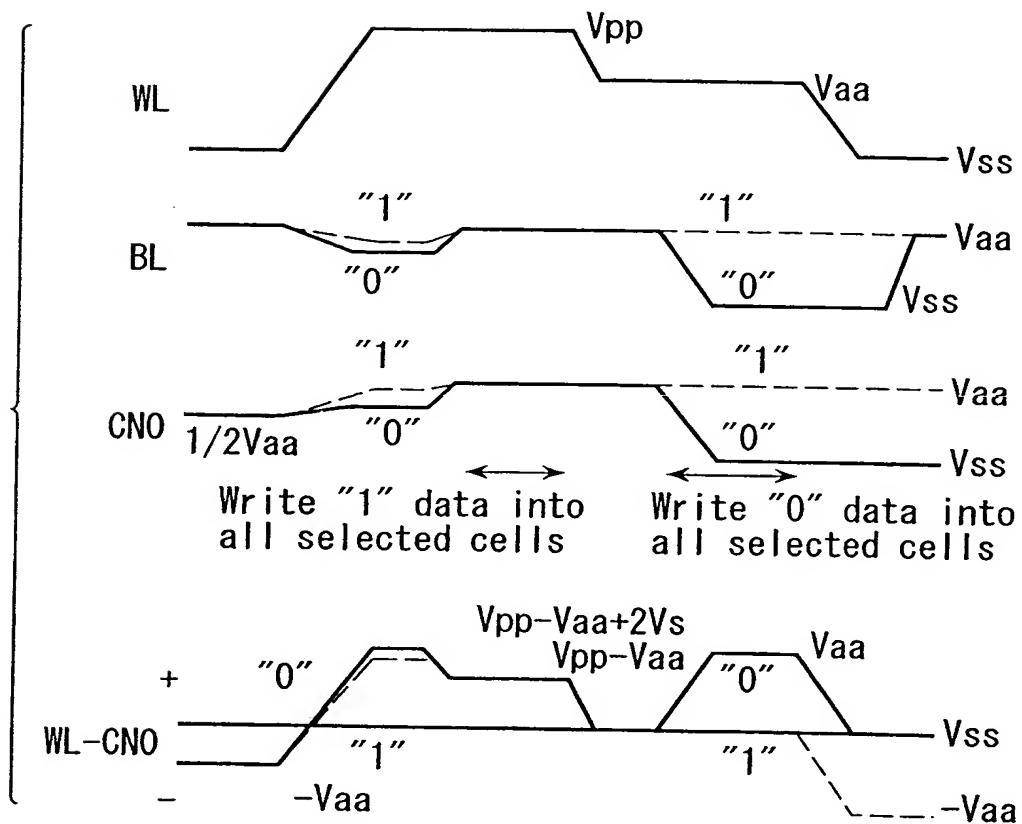
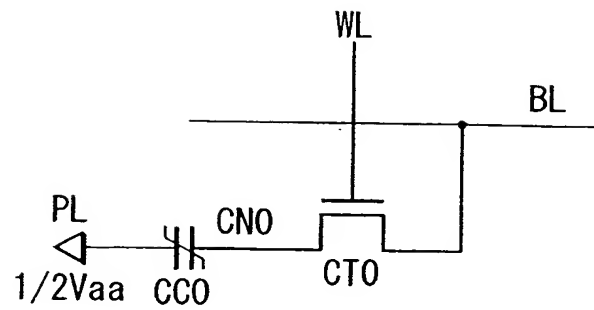


FIG. 8B

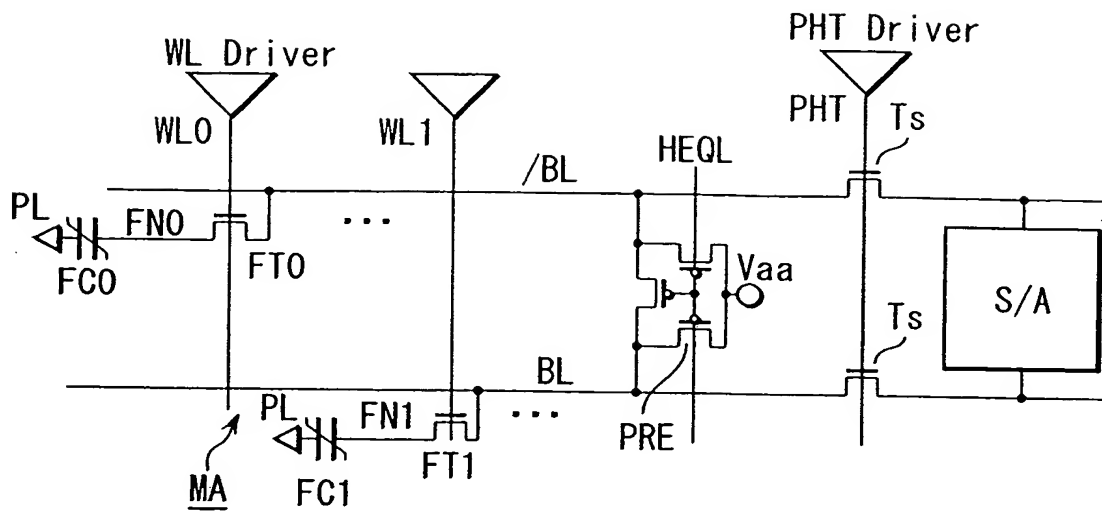


FIG. 9

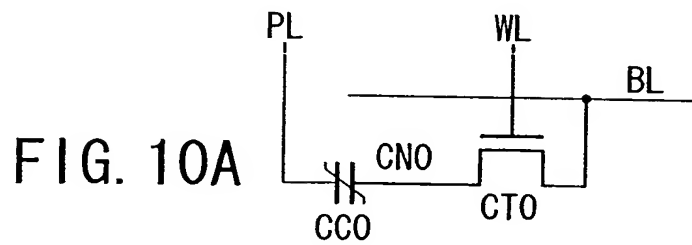
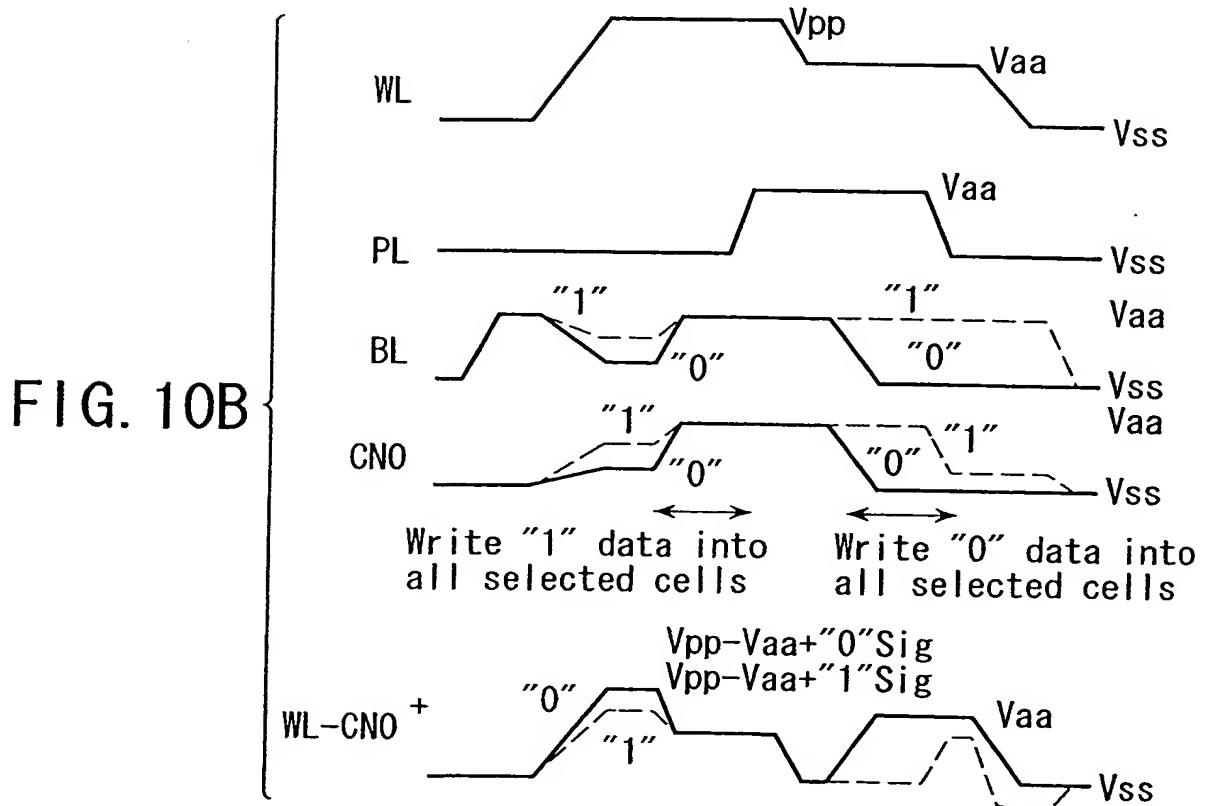


FIG. 10A



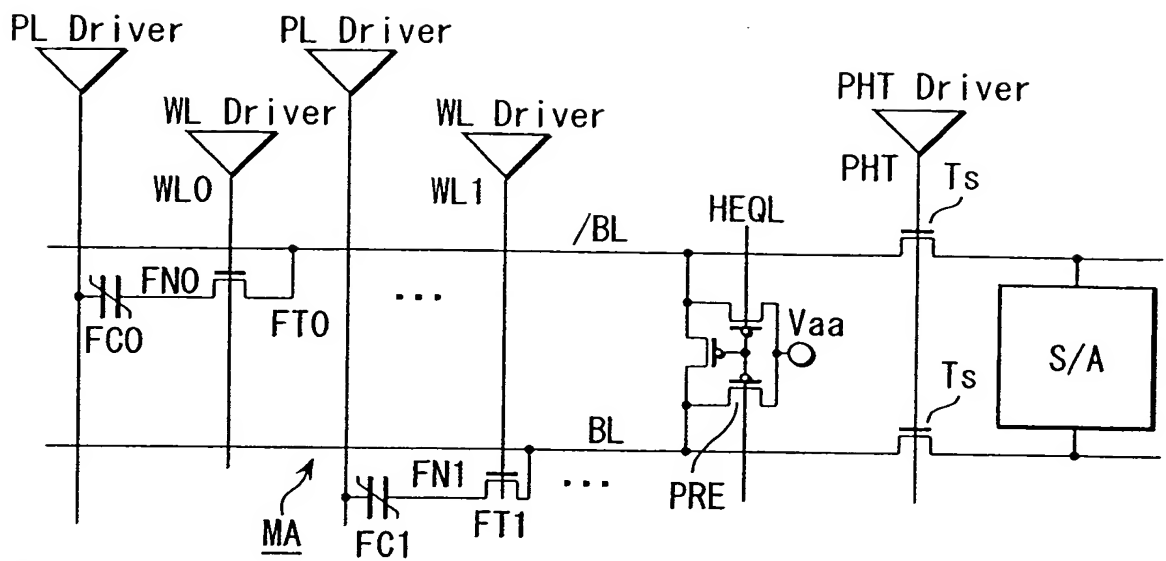


FIG. 11

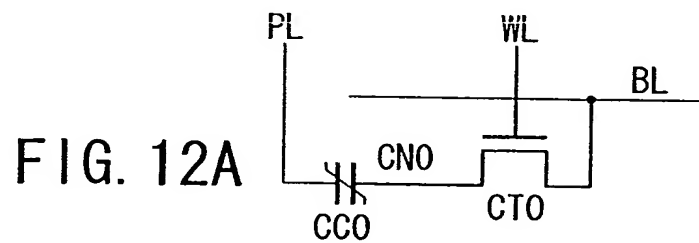


FIG. 12A

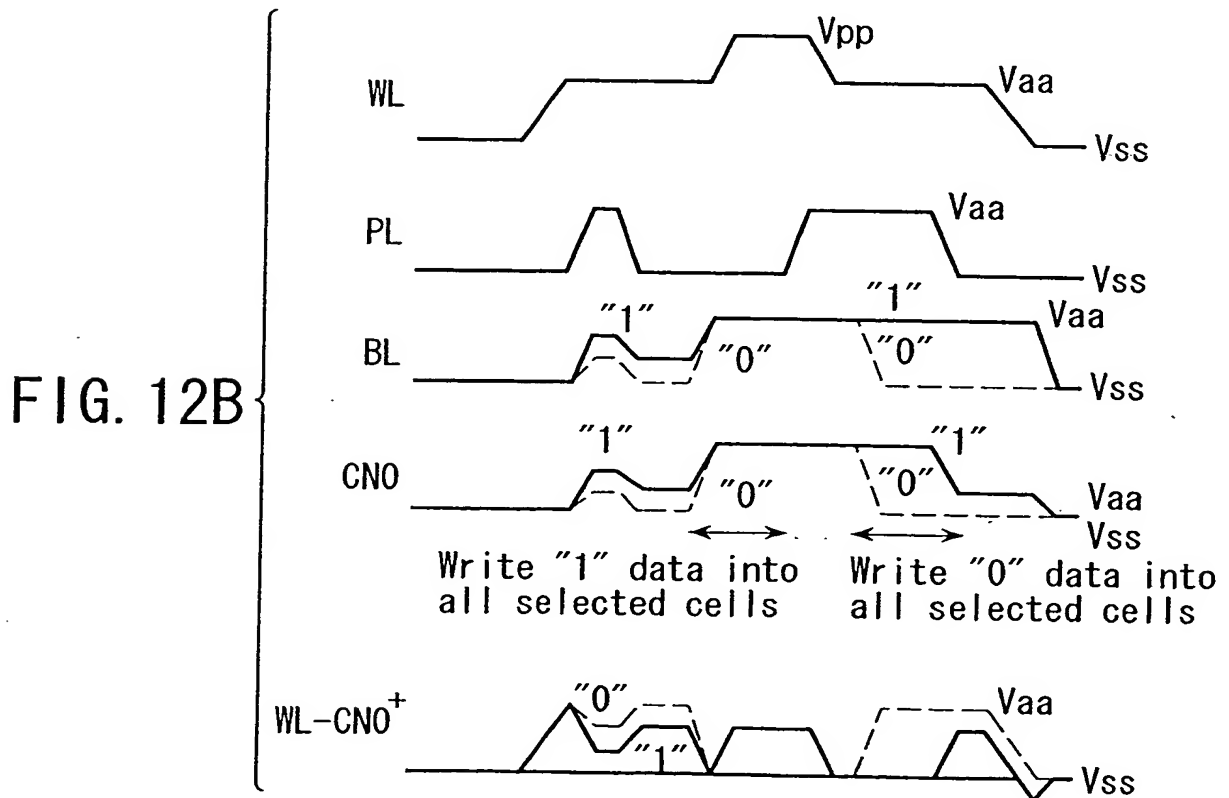
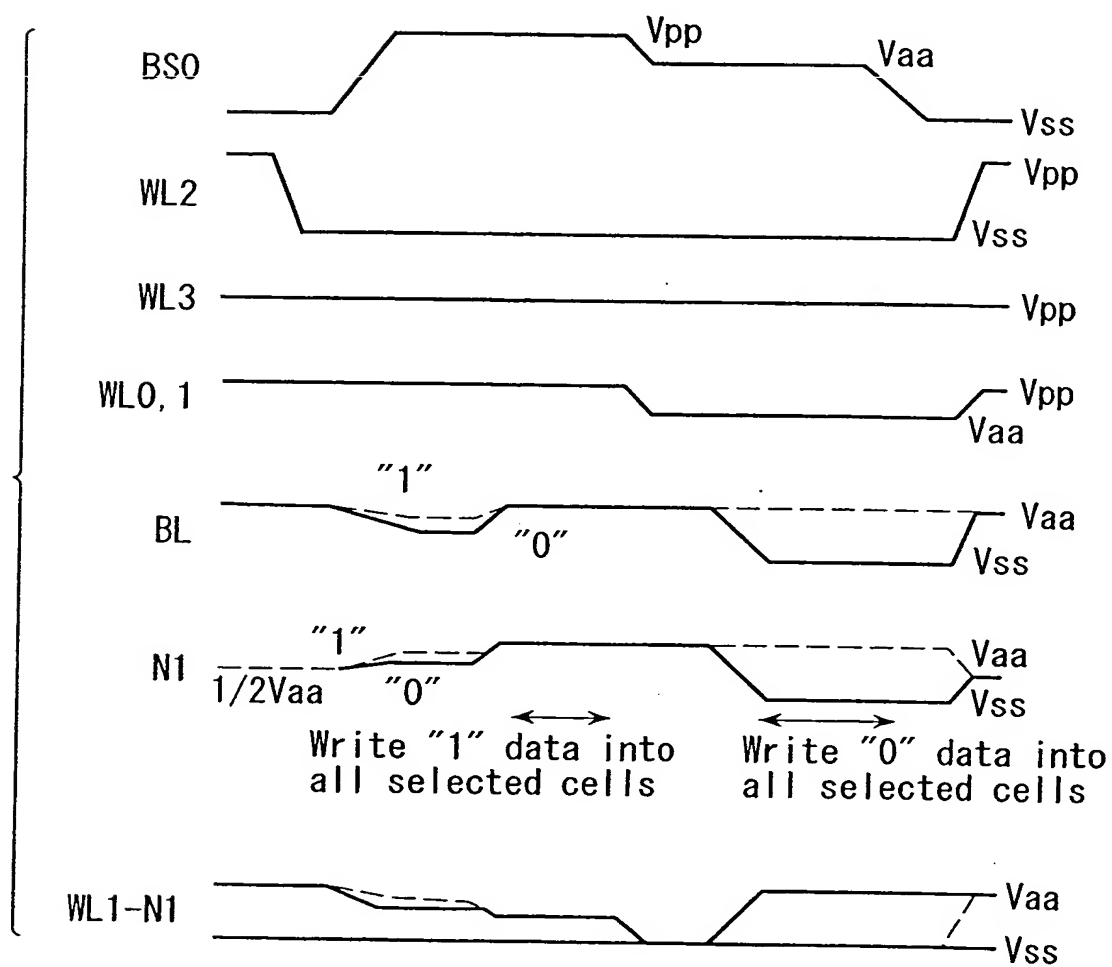
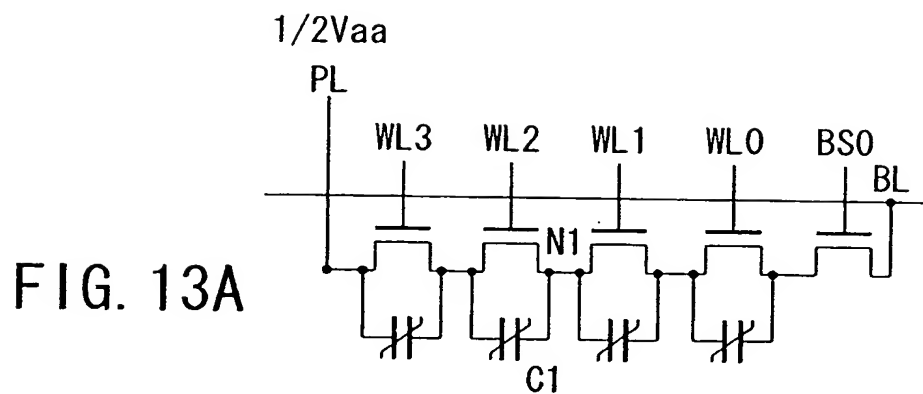
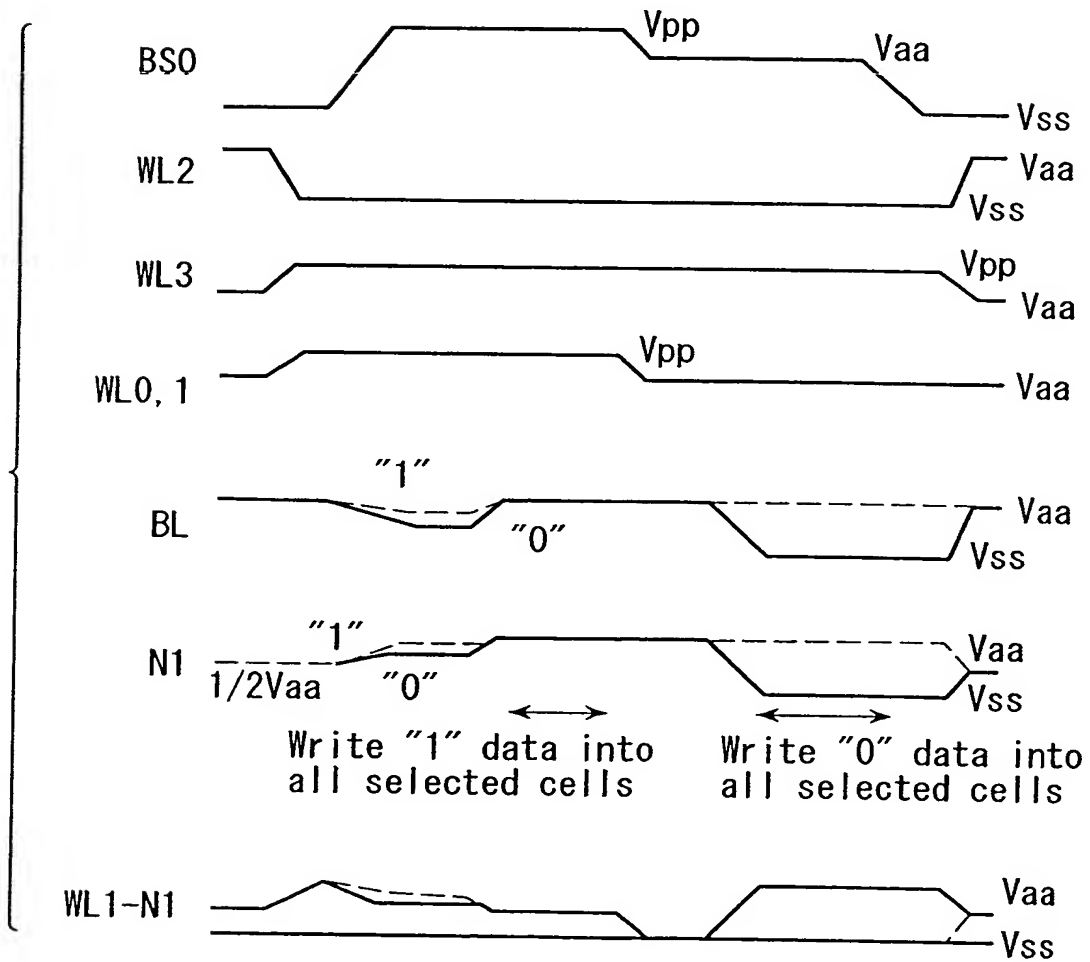
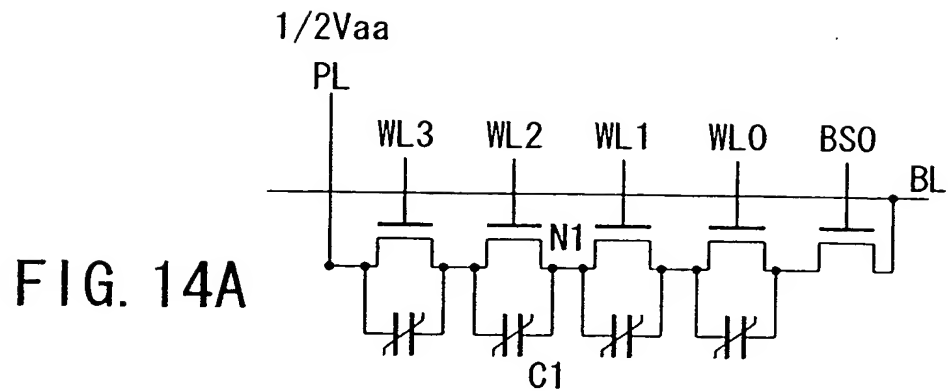


FIG. 12B





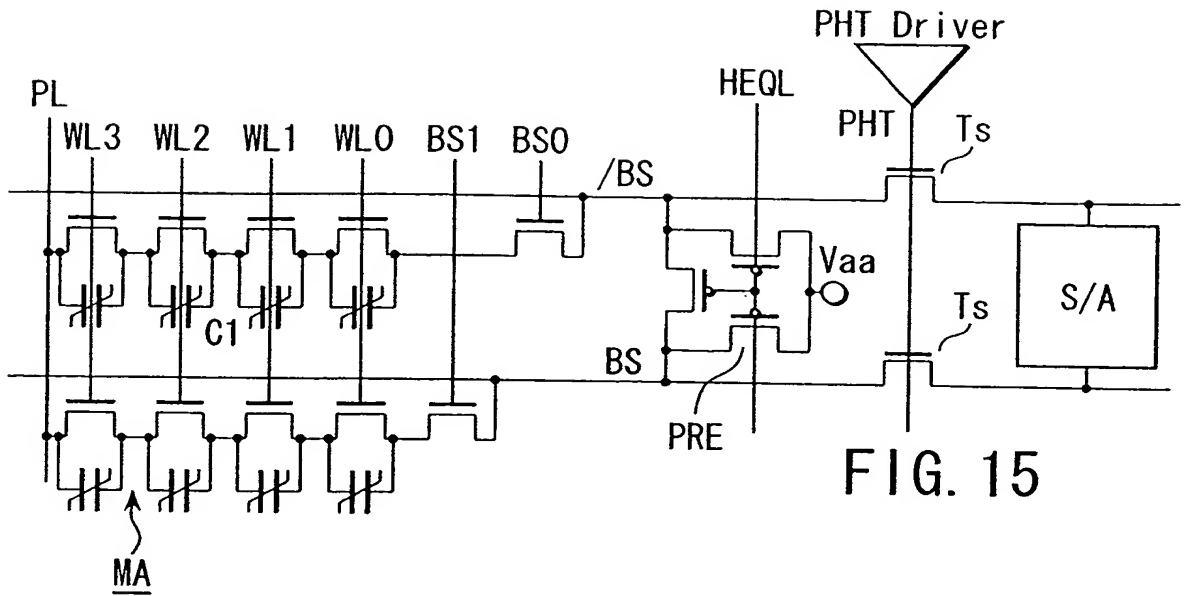


FIG. 15

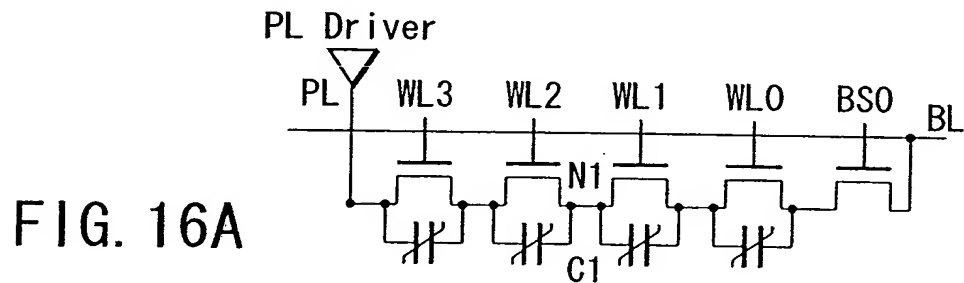


FIG. 16A

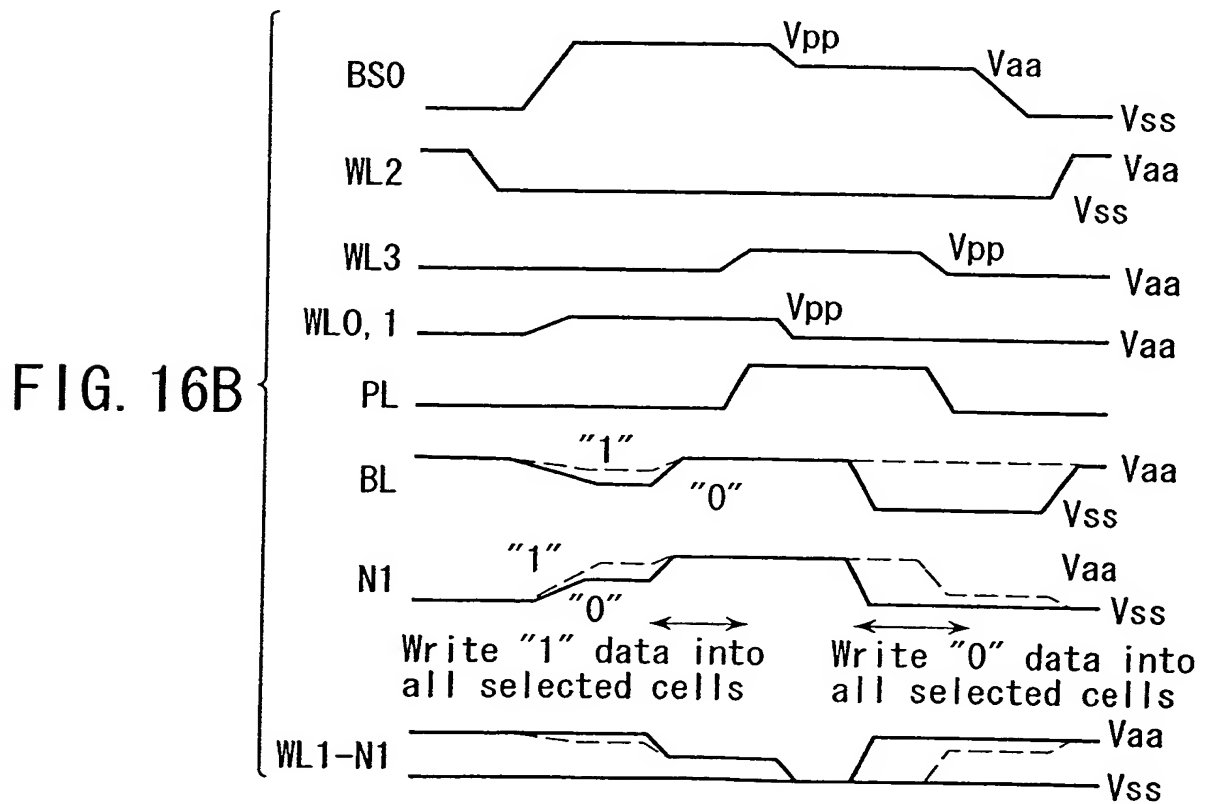
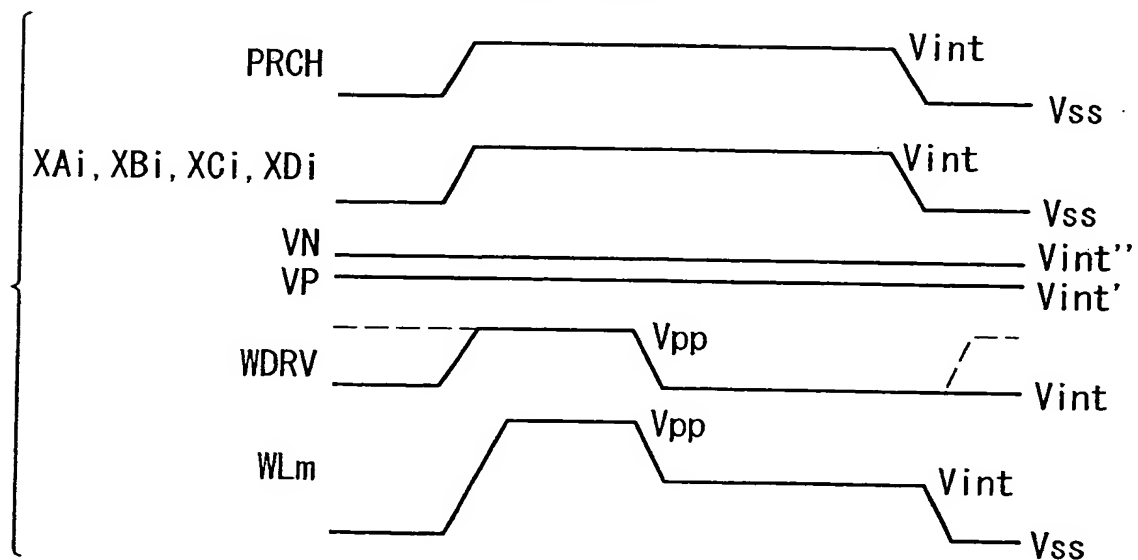
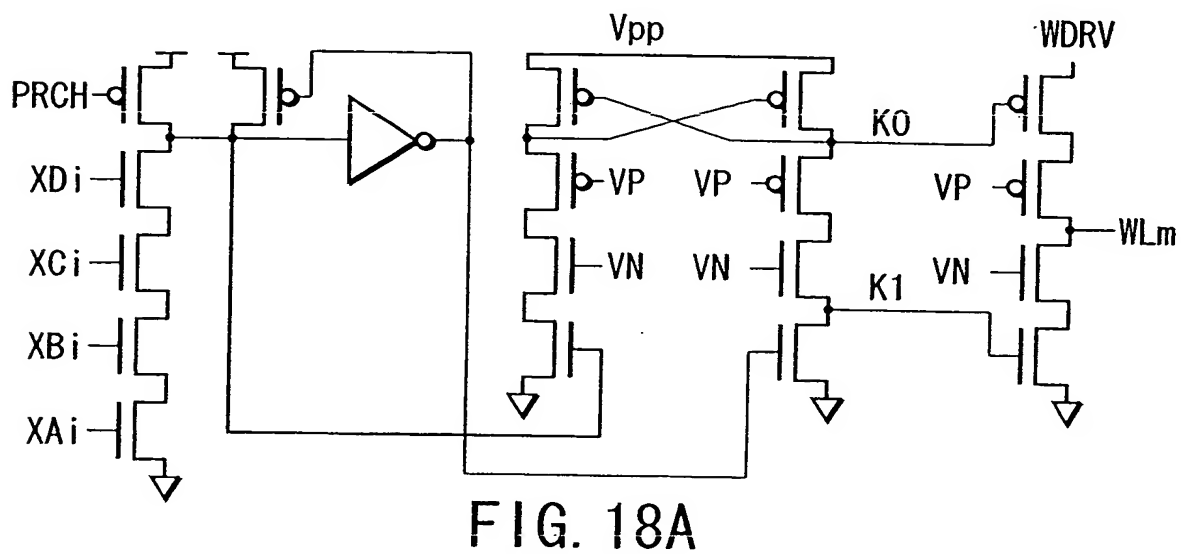
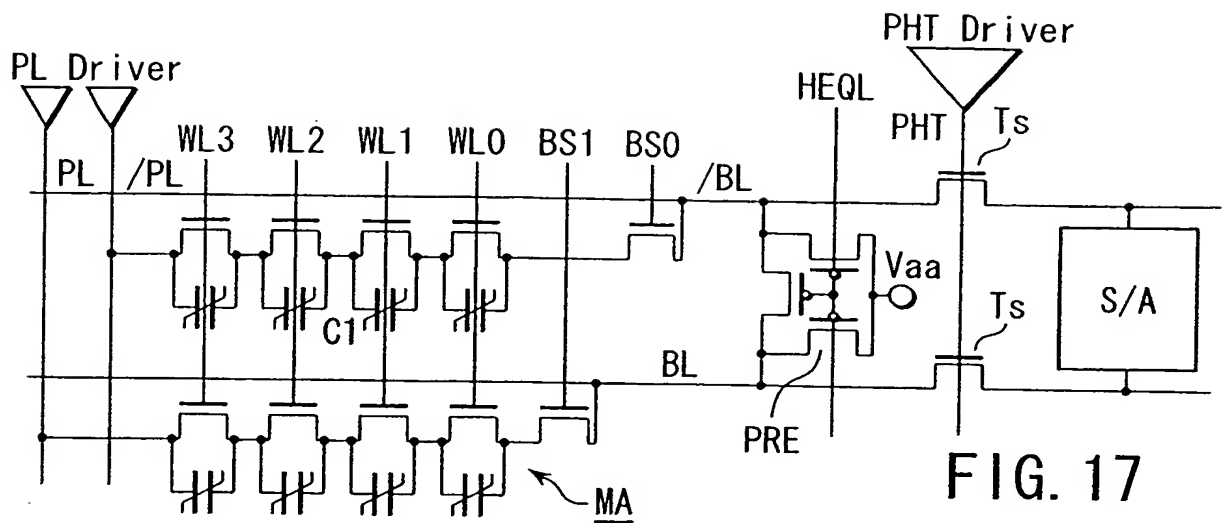


FIG. 16B



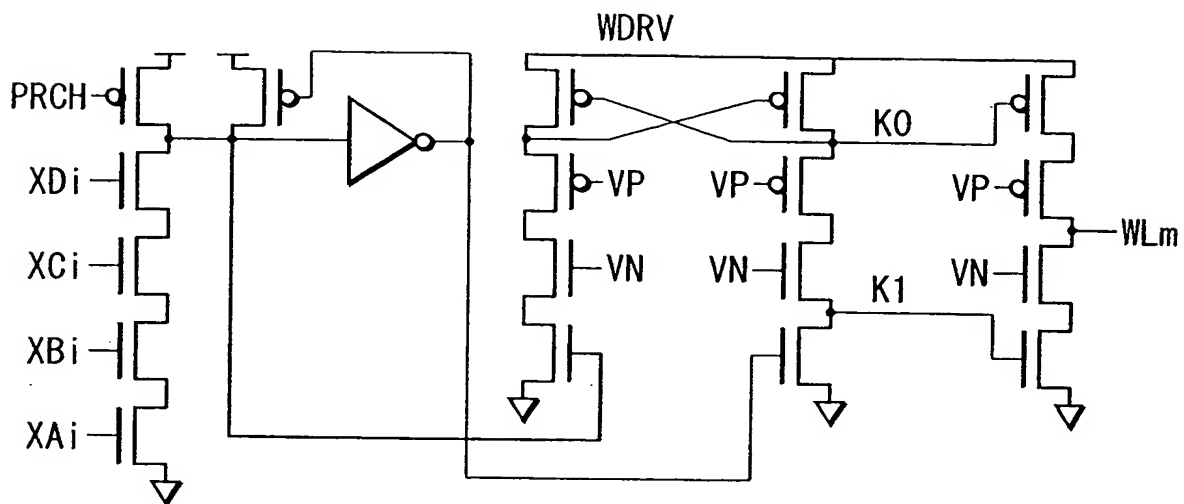


FIG. 19A

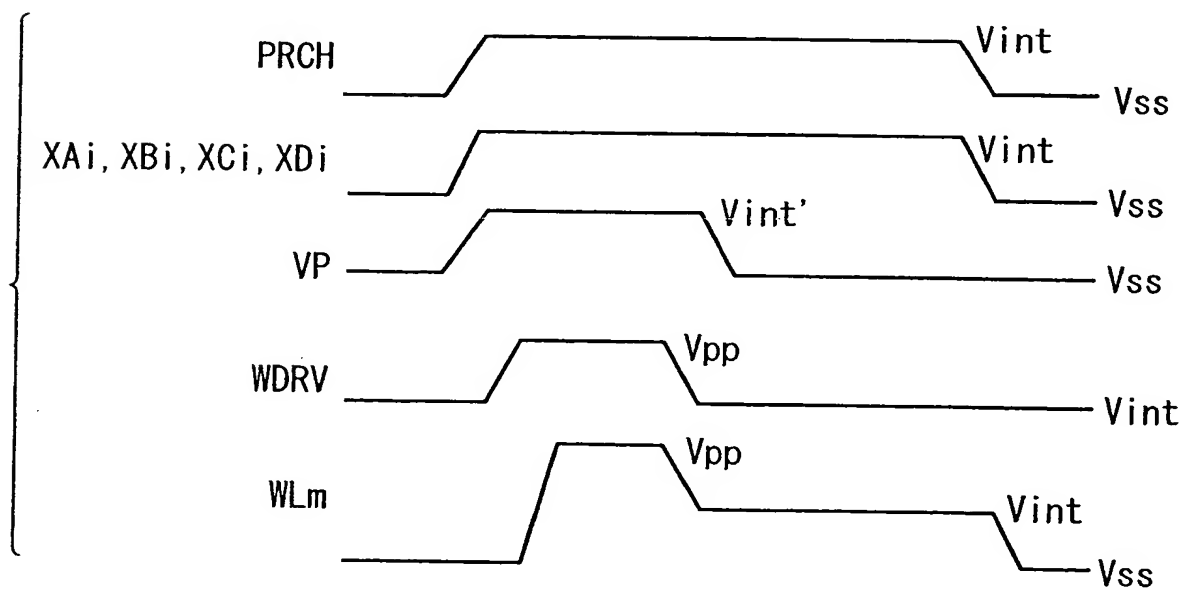


FIG. 19B

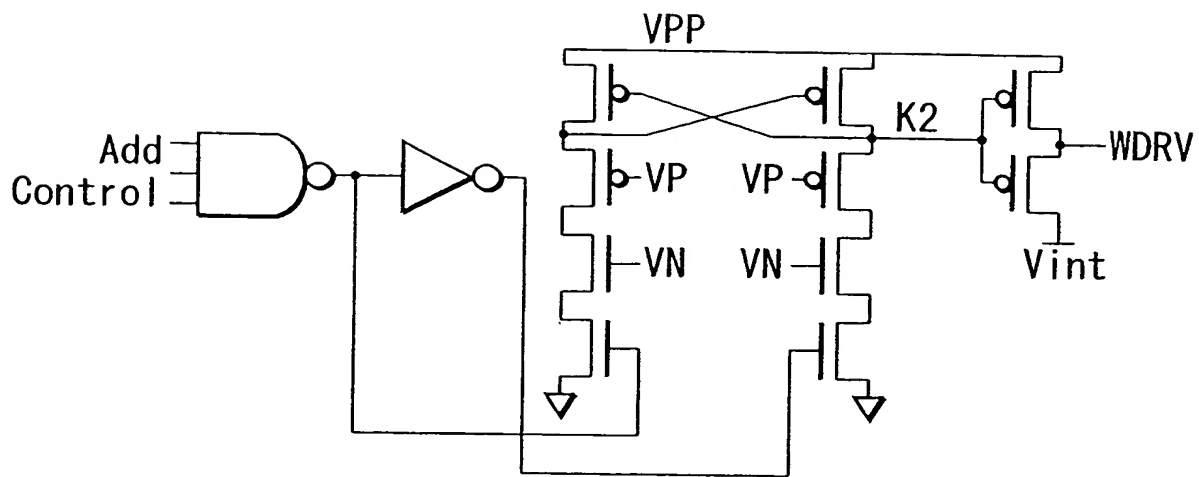


FIG. 20A

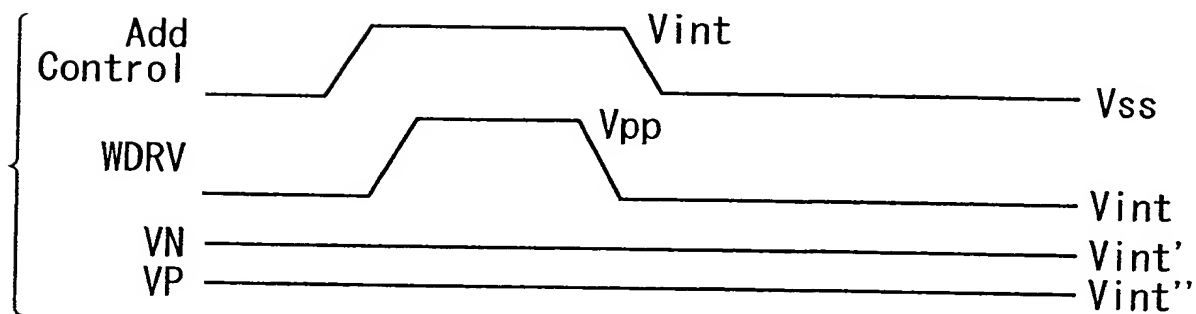


FIG. 20B

FIG. 21A

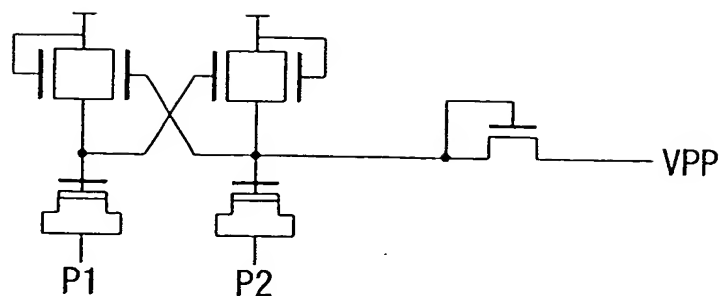


FIG. 21B

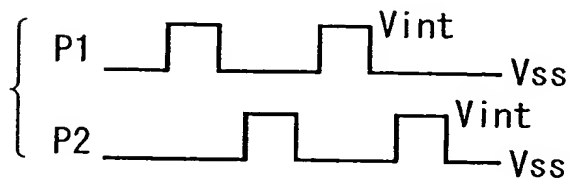


FIG. 22A

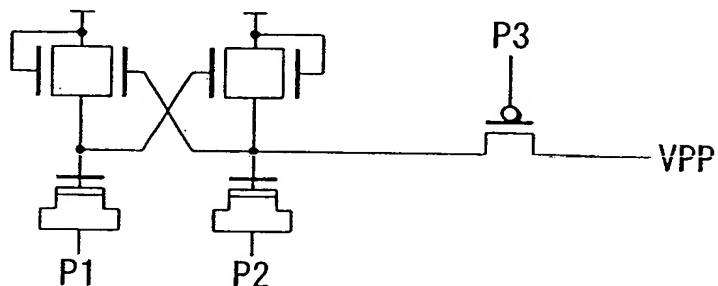


FIG. 22B

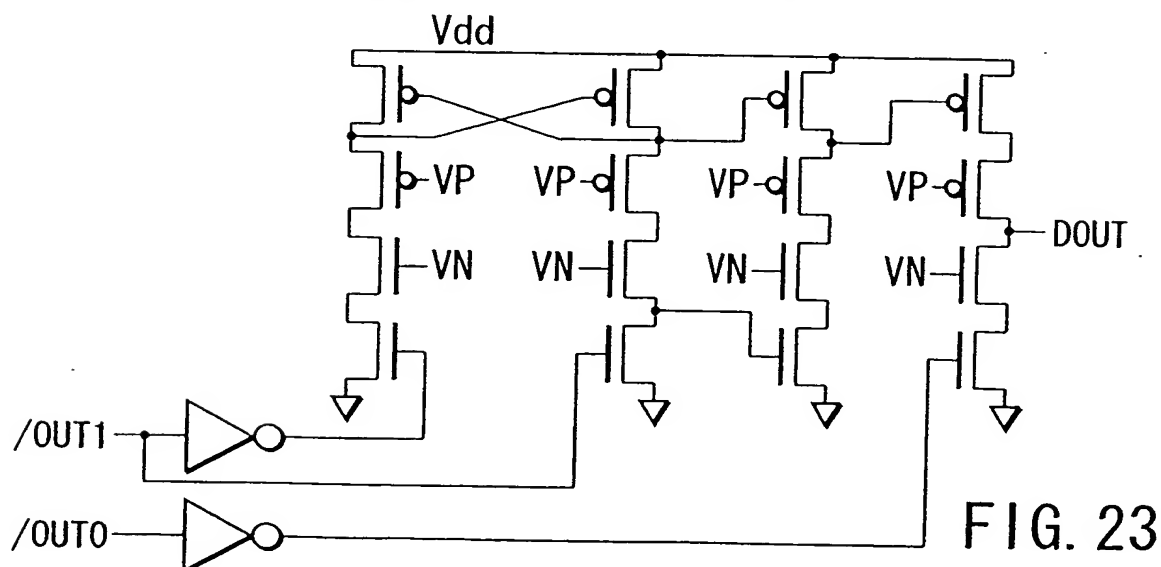
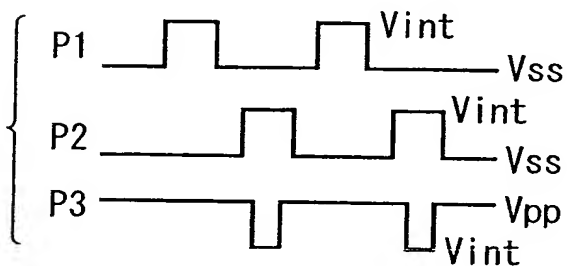


FIG. 24A

Logic	I/O 80A	Logic 50A	
DRAM	Cell 80A	Core 80A	Peri 50A

FIG. 24B

Logic	I/O 80A	Logic 50A	
DRAM	Cell 50A	Core 80A	Peri 50A

FIG. 24C

Logic	I/O 50A	Logic 50A	
DRAM	Cell 50A	Core 50A	Peri 50A

FIG. 25A

DRAM	Cell 80A	Core 80A	Peri 80A	I/O 80A
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FIG. 25B

DRAM	Cell 80A	Core 80A	Peri 50A	I/O 80A
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FIG. 25C

DRAM	Cell 50A	Core 80A	Peri 50A	I/O 80A
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FIG. 25D

DRAM	Cell 50A	Core 50A	Peri 50A	I/O 50A
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FIG. 26A

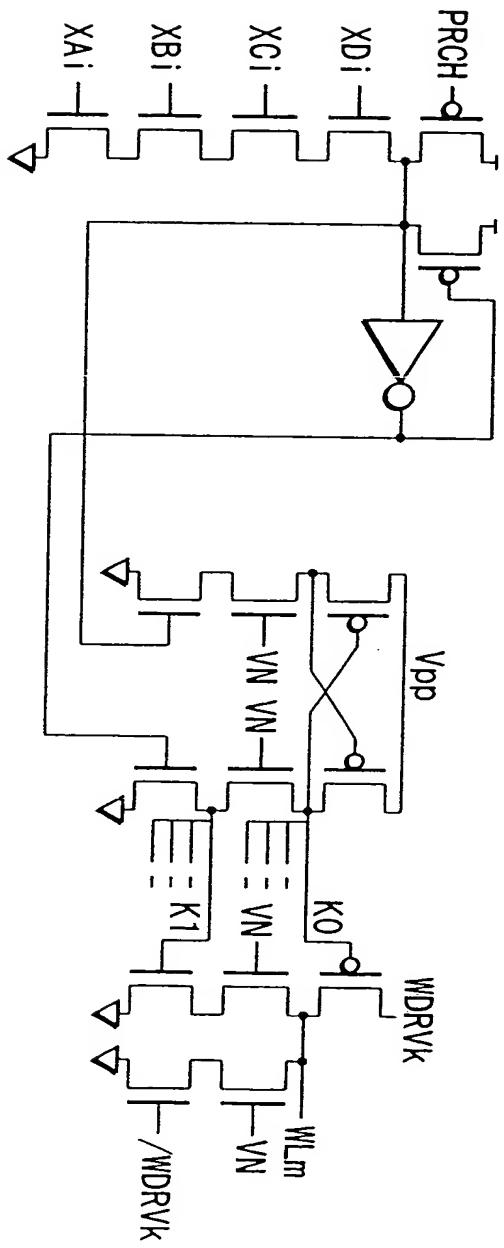
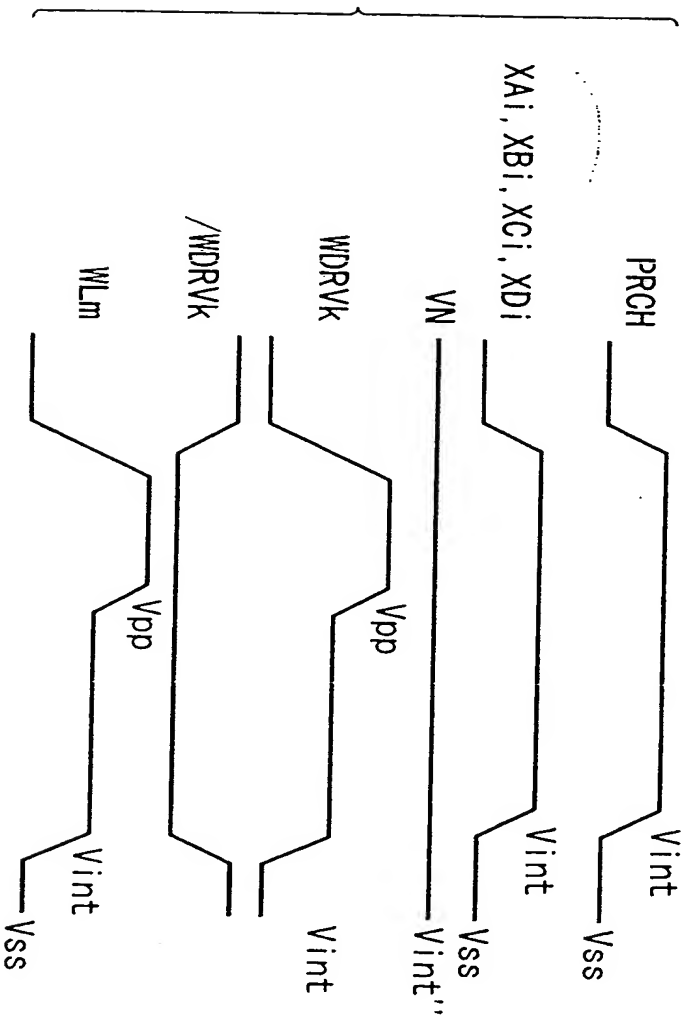


FIG. 26B



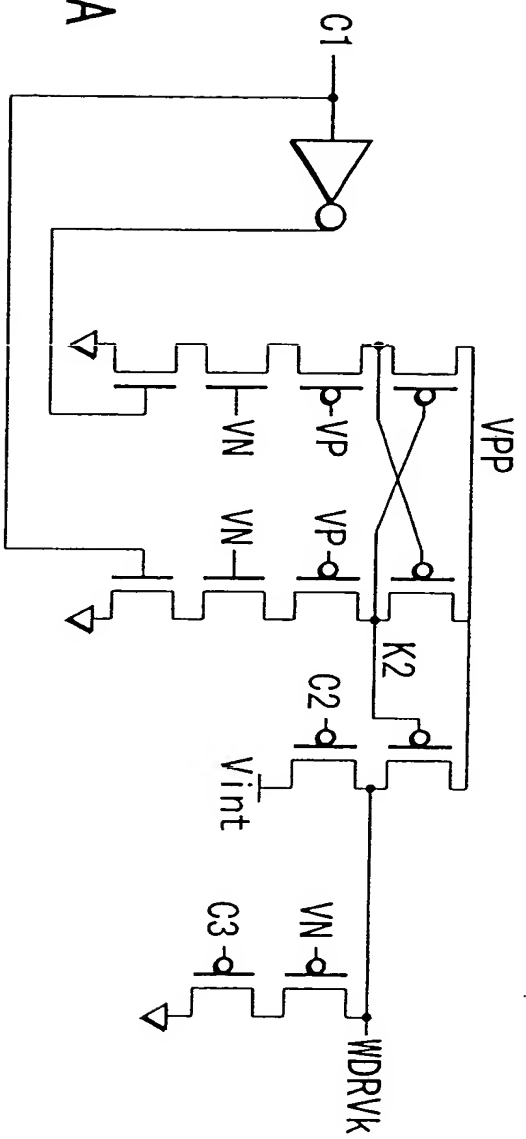


FIG. 27A

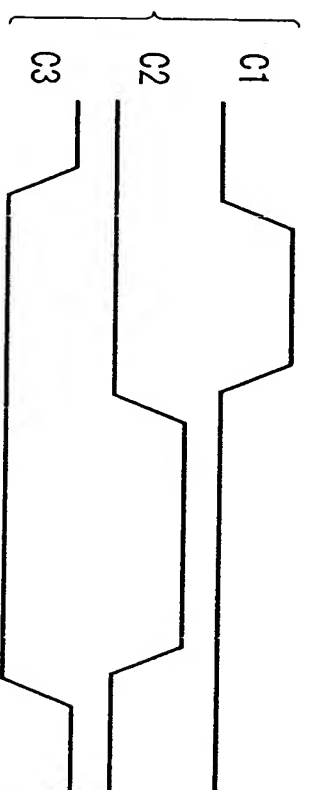


FIG. 27B

FIG. 28A

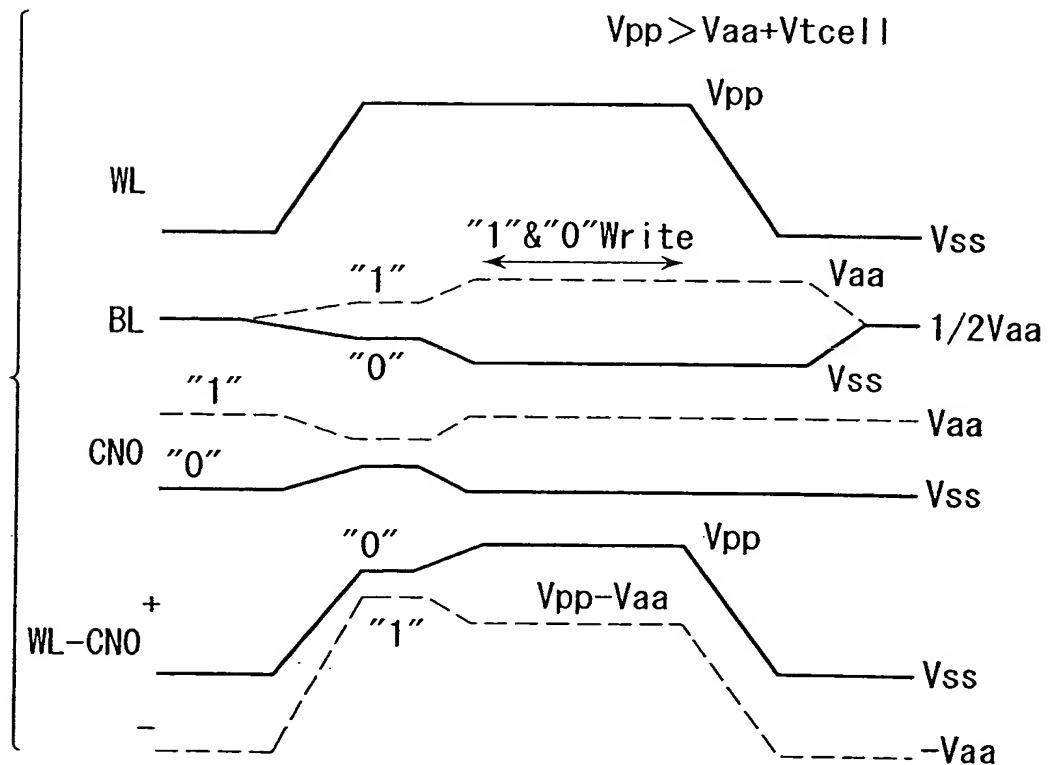
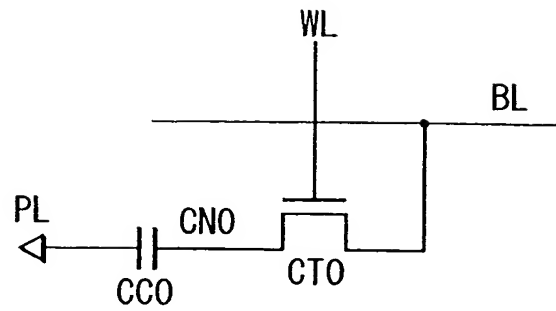


FIG. 28B

FIG. 29A

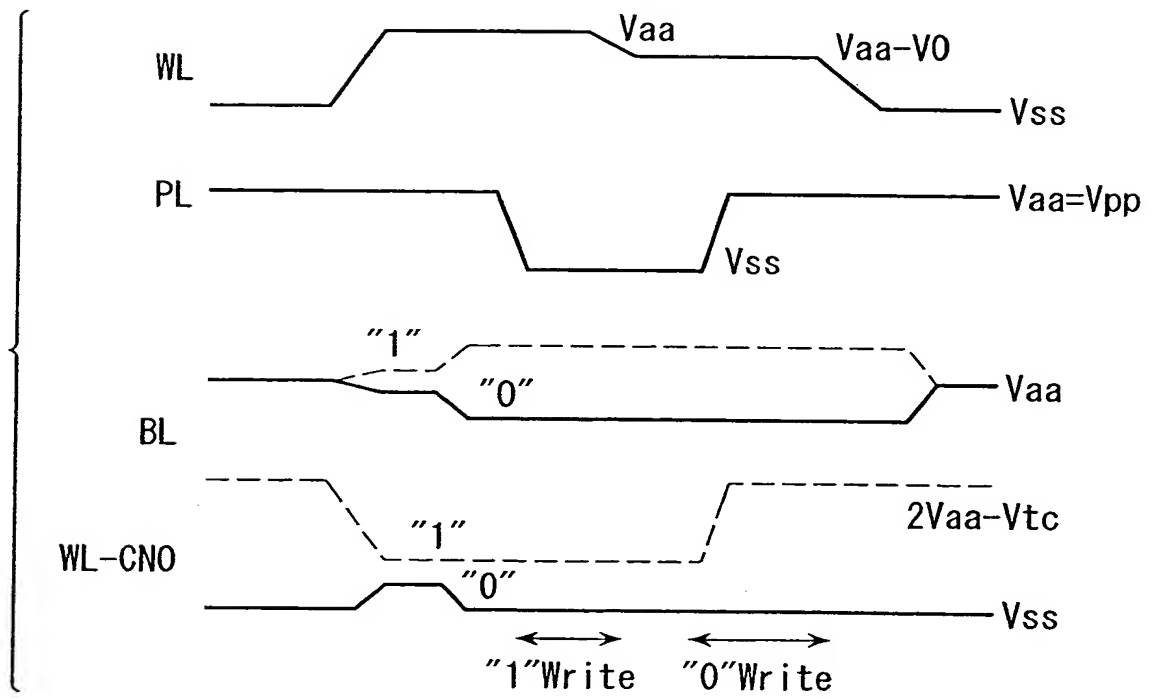
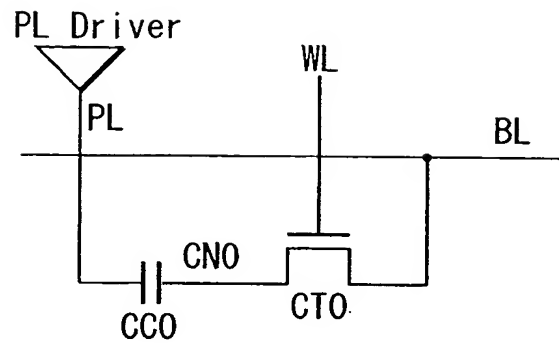


FIG. 29B